Column 8, lines 12-17. Endo is concerned with reducing writing and erasing voltages of EEPROMs and the endurance of such devices for write/erase cycles.

Nagata describes a MIS-FET device wherein dielectric layers are used to isolate adjacent devices. The Examiner cites Nagata for disclosing an equation regarding effective oxide thickness.

Independent claim 8 is prima facie not obvious over the cited references, because the references do not disclose a transistor having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate where the gate dielectric comprises a first dielectric material and a second dielectric material. The EEPROM substrate of Endo shows the two layer dielectric material formed between a floating gate and a control gate.

Applicant also believes there is no motivation from the cited references for the transistor of claim 8 as Endo is concerned with reducing read/write voltages and increasing the cycle life of the EEPROM. Endo does not suggest or teach increasing the current flow through a transistor by modifying a gate dielectric to increase its capacitance. Although voltage reduction are desired for reading and writing to EEPROMs, Endo focuses on modifying the intergate dielectric material. Application to the gate dielectric adjacent the substrate, according to the Applicant's reading, is

not addressed. Finally, Nagata, according to Applicant's understanding, only addresses isolation of adjacent devices and such teaching provides no motivation for modifying the gate dielectric of a transistor.

For the above stated reasons, claim 8 is not obvious over the cited art. Claims 9-14 depend from claim 8 and therefore contain all the limitations of that claim. For the reasons stated with respect to claim 8, claims 9-14 are not obvious over the cited references. Applicant respectfully requests the Examiner withdraw the rejection to claims 8-14.

New claim 15 relates to an apparatus comprising a substrate having a transistor device formed thereon, the transistor device having a gate dielectric disposed directly between a surface of the substrate and a gate electrode. Because the gate dielectric is disposed between the substrate and the gate electrode, the arguments presented above with respect to the cited art are equally applicable to claim 15. Claims 16-21 depend from claim 15 and therefore contain all the limitations of that claim. Applicant accordingly believes claims 15-21 are allowable over the cited art.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

Respectfully submitted,

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Date: 6/29/00

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on June 29, 2000.

Nedy Calderon 6/29/00

Nedy Calderon Date